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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/759,715	01/13/2001	Hiroaki Tsugane	15.31/5631	2451

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EXAMINER
MAGEE, THOMAS J

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/759,715	TSUGANE ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 15-29* is/are pending in the application.

4a) Of the above claim(s) *5-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 15-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *12* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections – 35 U.S.C. 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 15, 17, 18, and 23 – 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagai (US 6,104,053) in view of Owens et al. (US 4,598,460).

3. Regarding Claim 1, Nagai discloses a method for manufacturing a semiconductor device having a DRAM, including a cell capacitor (25,42,27) (Figure 17) and a capacitor element (20,7,6,31) formed in the analog (peripheral) region, whereby an impurity region in the DRAM region (12) is used to connect an electrode (25) of the capacitor and the doped region (33) used to connect the electrode (11) of the capacitor in the analog region. Nagai further discloses that the dielectric layer of the cell capacitor (42) and the capacitor element (42) are formed simultaneously (Col. 6, lines 17 – 29) and in like fashion, the cell plate (27) of the cell capacitor and the upper electrode (40) of the capacitor element are also formed simultaneously (Col. 6, lines 22 – 29).

Nagai does not disclose the simultaneous formation of the ion implanted impurity regions in the analog and memory region, however, the simultaneous doping of separate device regions by ion implantation is conventional (See Owens et al., Col. 8, lines 14 – 16) and utilized for more than two decades. Hence, it would have been obvious to one of ordinary

skill in the art at the time of the invention to perform simultaneous doping of the regions to reduce the number of processing steps. Further, the lower electrode (20) of the upper capacitor could also have been formed simultaneously with the formation of the storage node (25) of the cell capacitor and would have been obvious to one of ordinary skill in the art at the time of the invention to provide more efficient processing.

4. Regarding Claim 17, Nagai discloses the formation of a semiconductor device including a DRAM region and an analog region wherein an impurity region (33) is formed (Col. 12, lines 17 – 21) in the analog region, an interlayer dielectric layer (31) formed on the semiconductor substrate where the dielectric is between the substrate and capacitor element (11). Further, Nagai discloses forming a cell capacitor in the DRAM region (25,42,27) and an embedded connection layer (37,29) Figure 19) connecting the semiconductor substrate in the impurity region (33) and extending through the dielectric layer (15), whereby the embedded connection layer is positioned in a connection hole (Figures 2, 19) with one end connected to the impurity region and the other to the surface of the capacitor (Col. 13, lines 44 – 54). Nagai does not disclose connection at the bottom surface of the lower electrode, but rather the top surface of the upper electrode. However, it has been ruled that where functional equivalence is maintained, rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86, USPQ 70.

5. Regarding Claim 18, Nagai discloses formation of an additional capacitor element (33, 31, 43) and an additional embedded connection layer (42,39) where the layer extends from the additional capacitor to the impurity region and serial connection of the two

capacitors is provided through the impurity region.

6. Regarding Claims 23 - 26, Nagai does not disclose the thicknesses of dielectric layers, 31 and 42, but capacitor insulating layers are known to be extremely thin, as shown in the figures. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to utilize an equivalent thickness for each of the layers, since it has been held that where the general conditions are disclosed in the prior art, discovering the optimal value involves only routine skill in the art. In re Aller, 105 USPQ 233.

7. Regarding Claim 27, Nagai disclose forming an additional capacitor (26,42,27) in the DRAM region.

8. Regarding Claim 28, Nagai discloses simultaneously forming the storage node of the cell capacitor (25) (Figure 14) and the additional storage node (26) of the additional cell capacitor, simultaneously forming the lower electrode of the capacitor element and additional capacitor element (Figure 9), simultaneously forming the dielectric layer of the cell capacitor (42, Figure 15) and the dielectric layer of the additional cell capacitor (42), simultaneously forming the dielectric layer (31) of the capacitor element and the additional capacitor element, simultaneously forming the cell plate (27) of the cell capacitor and additional cell capacitor, and simultaneously forming the upper electrode of the capacitor element and additional capacitor element (Figure 9).

9. Claims 2 – 4 and 19 – 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagai, as applied to Claims 1,15,17,18, and 23 – 29 above, and further in view of

Choi et al. (US 6,040,596).

10. Regarding Claims 2, 3, 19, and 20, Nagai does not disclose the formation of resistance elements in the analog region. Choi et al. disclose the fabrication of a device with DRAM and peripheral circuit regions containing capacitors and resistors in the analog region. Choi et al. disclose the formation of a first and second resistance element (Figure 5A), where the sheet resistance of the two is adjusted by varying the impurity concentration introduced into the polysilicon (Col.5, lines 62 – 65). It would have been obvious to one of ordinary skill in the art at the time of the invention to alter the relative impurity concentrations of the two resistance elements to produce a lower resistance in the first element, since it has been held that discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. Nagai further discloses that the cell plate of the capacitor (38) and the electrode of the resistor (38) are the same and hence are formed simultaneously (Col. 5, lines 45 – 50).
It would have also been obvious to one of ordinary skill in the art at the time of the invention to combine Choi et al. with Nagai to obtain resistance elements in the analog region in order to complete the analog circuit for a functioning device.

11. Regarding Claims 4, 21 and 22, Nagai does not disclose the formation of resistors or the use of silicide layers. Choi et al. disclose (Figure 1B) the formation of a silicide layer (29b) on the polysilicon layer (29a) of the resistor. Since the resistance of the polycide layer is lower than that of the polysilicon (Col. lines 56 – 65), it would have been obvious to one of ordinary skill in the art at the time of the invention to deploy a polycide in the

first resistance element to produce a low sheet resistance value relative to the second.

Response to Arguments

12. Applicant's arguments have been carefully considered but are regarded as moot in terms of the new ground(s) of rejection. Further, Applicant appears to have used the argument that formation of elements within the DRAM and analog region "simultaneously" is novel. However, this is a notoriously well known procedure, deployed routinely in the art (See Nagai and Choi et al., Col. 1, lines 24 – 29).

Conclusions

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(703) 305 5396.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Tom Thomas**, can be reached on **(703) 308-2772.**. The fax number for the organization where this application or proceeding is assigned is **(703) 308-7722.**

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Thomas Magee
February 12, 2003